DMARD08 ±3g Tri-Axial Digital Accelerometer

General Description

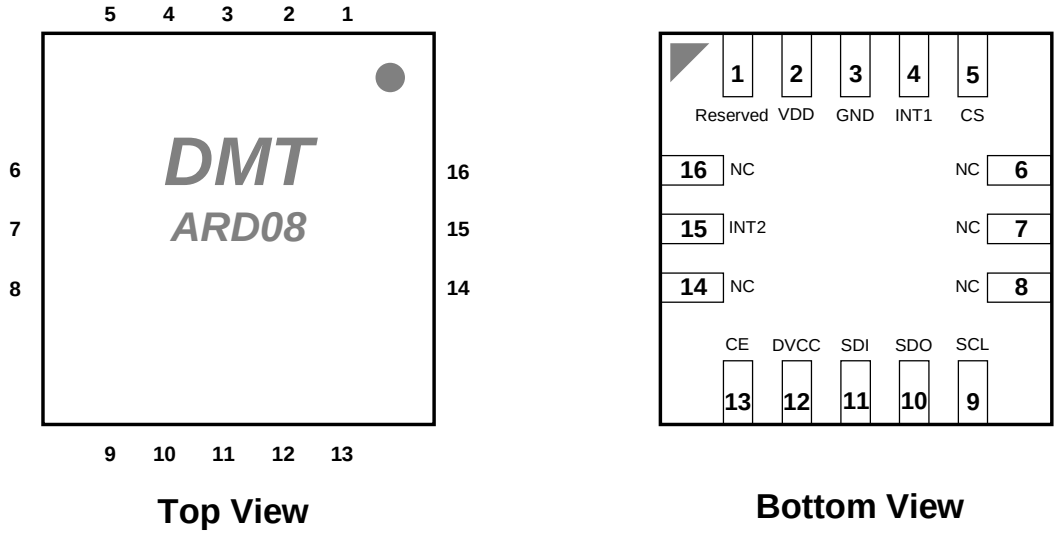
DMARD08 is a ±3g tri-axial digital accelerometer embedded with 11-bit ADC and in small 3×3×1 mm^3 form-factor. DMARD08 contains in a compact plastic LGA package a sensing element and a conditioning CMOS IC. The sensing element is a MEMS device by proprietary piezoresistive technology. The CMOS IC provides SPI and I2C digital interface and interrupt signals with build-in functionality. DMARD08 can be deployed without further user interference in many applications.

Features

- Tri-axial digital accelerometer with ±3g dynamic range
- 11 bit ADC embedded with SPI (4-wire) and I2C digital interface
- Temperature sensor for internal compensation and capable of digital output
- Low operation voltage of +2.4V ~ +3.6V with minimum interface voltage of +1.7V
- Low power consumption (Operation: typical 250uA@3V, Stand-by: Max. 5uA)
- Two interrupt pins configurable from three interrupt sources: freefall, click and high-G
- Freefall detection with user settable threshold
- 6-direction click detection with user settable threshold
- 3-direction motion detection (high-G) with configurable logic combination and threshold setting
- User selectable bandwidth and pin-controllable standby mode
- 5000g shock tolerance
- 16-pin LGA package with RoHS compliance and lead-free. Footprint 3mm×3mm, height 1mm.

Applications

Display orientation switching, click sensing, menu scrolling, HDD protection, mobile phone, gaming, smart toys, etc.



Top View **Bottom View**

Figure 1: DMARD08

Domintech Co., Ltd. Tel: +886-2-2290-1288 Fax: +886-2-2290-1266 http://www.domintech.com.tw

Specifications

Table 1: Pin Descriptions

Pin	Name	Description	Pin	Name	Description
1	Reserved	Reserved	9	SCL	Serial interface clock
2	VDD	Analog power	10	SDO	Serial data interface
3	GND	Ground	11	SDI	Serial data interface
4	INT1	Interrupt signal 1	12	DVCC	Digital power
5	CS	Serial interface mode select	13	CE	Control of chip enable
6	NC	No connection inside	14	NC	No connection inside
7	NC	No connection inside	15	INT2	Interrupt signal 2
8	NC	No connection inside	16	NC	No connection inside

Table 2: General Specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage V_{op} (VDD)	T_a = -40℃ ~ +85℃	2.4	3.0	3.6	V
Interface Voltage DVCC	T_a = -40℃ ~ +85℃	1.7	—	3.6	V
Operating current I_{op}	V_{op} = 3V, T_a = 25℃	—	250	400	uA
Standby current I_{stby}	V_{op} = 3V, T_a = 25℃	—	3	5	uA
Dynamic range		—	±3	—	g
Sensitivity	V_{op} = 3V, T_a = 25℃	230	256	280	LSB/g
Zero-g offset	V_{op} = 3V, Ta = 25℃	—	±120	—	LSB
Sensitivity to temp. dependency	T_a = -40℃ ~ +85℃	—	±0.08	—	%/℃
Zero-g offset temp. dependency	T_a = -40℃ ~ +85℃	—	±2	—	mg/℃
Nonlinearity		—	±2	—	%FS
Cross axis sensitivity		—	2	—	%
Turn on time	N: average order	T_{ms} × N			ms
Noise	BW=100Hz	—	11	—	mg rms
Operation temperature T_a		-40	—	+85	℃
Storage temperature range		-40	—	+125	℃
Internal sampling period T_{ms}	User selectable	1.462, 2.925			ms
Internal sampling rate $1/T_{ms}$	User selectable	342, 684			Hz

Detection response time	User selectable	T_{ms}			ms
Bandwidth	Mechanical	DC	100	—	Hz
	Electrical	See Bandwidth Table 8			Hz
Freefall threshold	Default	—	523	—	mg
	Settable @ 7.8mg step	7.8	—	996	mg
Click threshold	Default	—	2.0	—	g
	Settable @ 250mg step	0.25	—	3.0	g
Temperature sensor sensitivity	V_{op} = 3V	—	16	—	LSB/℃
Temperature sensor accuracy	T_a = -40℃ ~ +85℃	—	±3	—	℃
Digital interface		I2C and SPI (4-wire)			
I2C clock frequency		—	—	400	kHz
Low level input voltage	CS, CE, SCL, SDI, SDO	-0.3	—	$0.2\times V_{if}$	V
High level input voltage	CS, CE, SCL, SDI, SDO	$0.8\times V_{if}$	—	$V_{if}+0.3$	V
Low level output voltage	INT, SDI, SDO	—	—	$0.1\times V_{if}$	V
High level output voltage	INT, SDI, SDO	$0.9\times V_{if}$	—	—	V

Maximum Ratings

Table 3: Absolute Maximum Rating

Parameter	Rating
V_{op}-GND	-0.3 ~ 4 V
Any other pin voltage	GND-0.3 to V_{op}+0.3 V
Temperature Range (Storage)	−40℃ to +125℃
ESD	2000V (HBM)
Acceleration (Any Axis, unpowered)	5,000 g
Freefall on concrete surface	1 m

Note: Stress above the absolute maximum rating as listed in Table 3 may cause permanent damage to the device

Connection Diagram

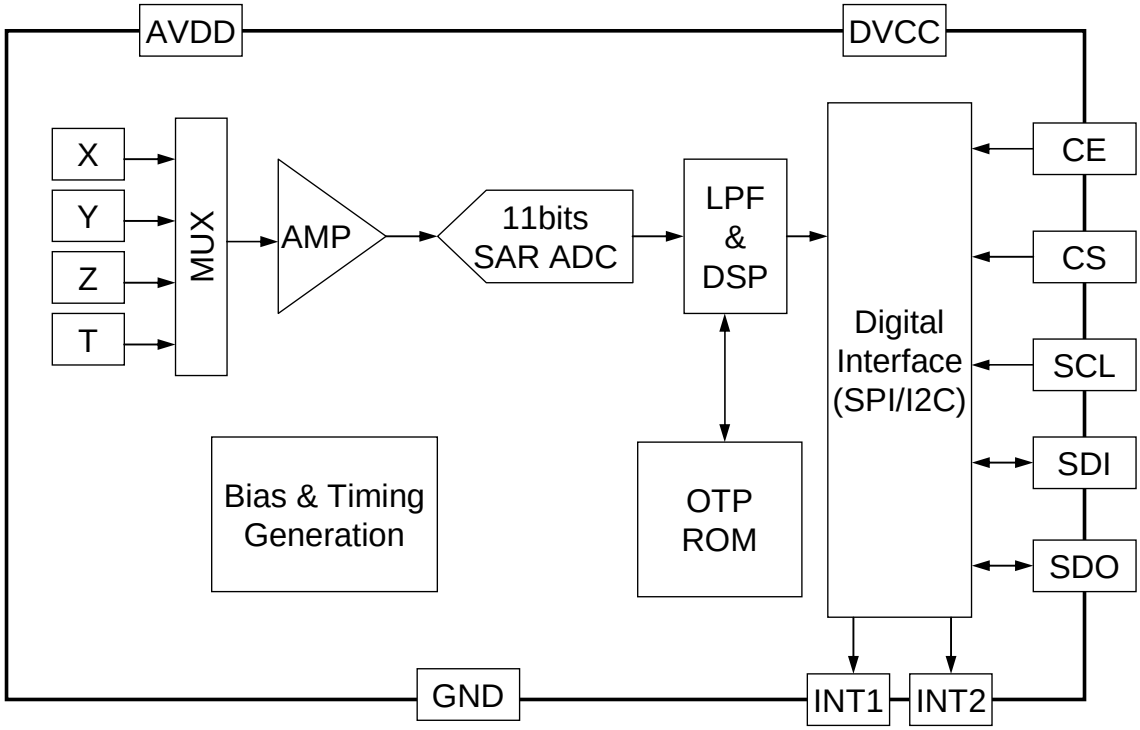


Figure 2: Block Diagram of DMARD08

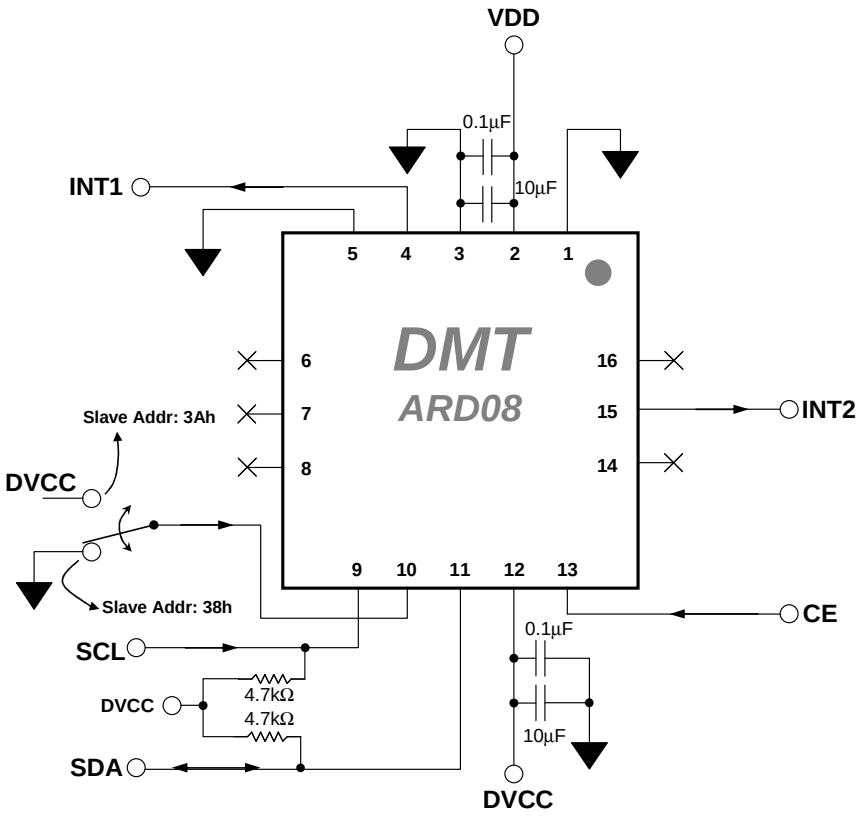


Figure 3: I2C Connection Example

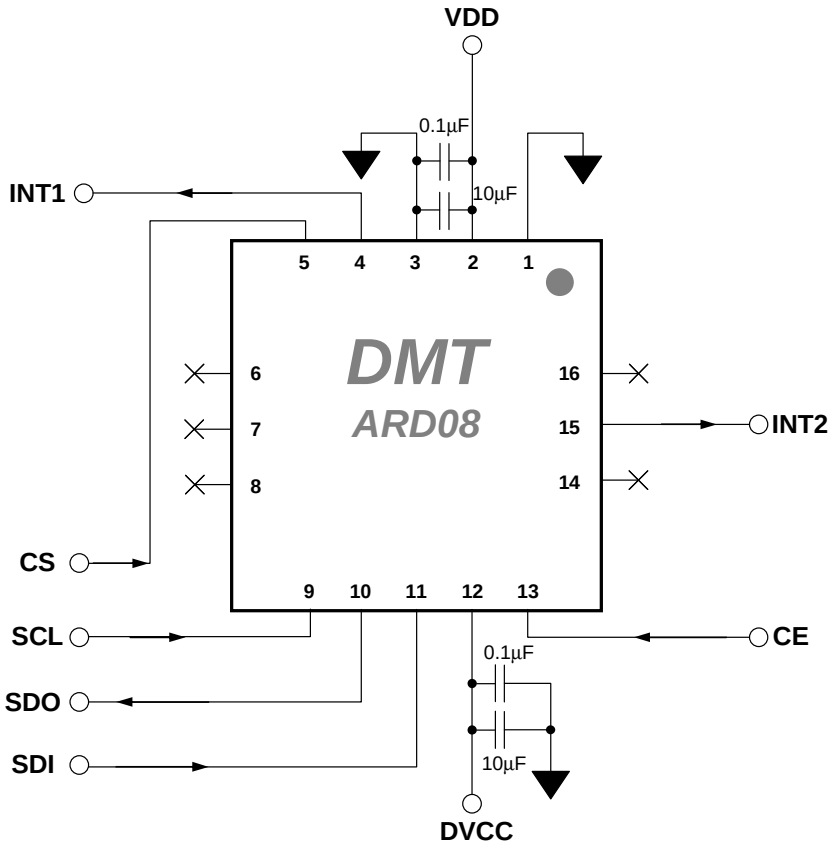


Figure 4: SPI Connection Example

User Registers

End users can read sensor outputs, control sensor behaviors and query the interrupt status by accessing the user registers. DMARD08 provides two digital interfaces, i.e. SPI 4-wire and I2C, for easy accessing these registers. The registers primarily consist of three categories: data, control and interrupt status registers. Sensor output values can be read from the data registers. The sensor behavior can be configured by setting up respective control registers. And lastly when using the build-in interrupt functions, the interrupt status registers bear state bits detailing interrupt event.

User Register Map

Table 4: User Register Map Table

Register Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default Value
Data Registers										
00h	Tout[10:3]								Read	NA
01h	Not used					Tout[2:0]			Read	NA
02h	Xout[10:3]								Read	NA
03h	Not used					Xout[2:0]			Read	NA
04h	Yout[10:3]								Read	NA
05h	Not used					Yout[2:0]			Read	NA
06h	Zout[10:3]								Read	NA
07h	Not used					Zout[2:0]			Read	NA
Control Registers										
08h	I2CFG[1:0]		I1CFG[1:0]		HGL	Tms	N[1:0]		Read/Write	00h
09h	HGAO	HGXEn	HGYEn	HGZEn	Not used	CLXEn	CLYEn	CLZEn	Read/Write	00h
0Ah	HGth[3:0]				FFth[3:0]				Read/Write	88h
0Bh	Not used				Clickth[3:0]				Read/Write	08h
Interrupt Status Registers										
0Ch	FFInt	HGInt	XHGP	XHGN	YHGP	YHGN	ZHGP	ZHGN	Read	NA
0Dh	Not used	CLInt	XCLP	XCLN	YCLP	YCLN	ZCLP	ZCLN	Read	NA

Note: SPI register address is 13-bit wide while I2C register address is 8-bit wide. For the same register, taking address 04h as an example, SPI address should be set as 0000000000100b, and I2C address should be set as 00000100b.

Data Registers

Temperature and acceleration output values can be read from the data registers. The sensor output is converted to an 11-bit value and stored across two register bytes. Data representation is 2's complement, i.e. MSB 1 means negative values. Data is periodically updated with sampling period which is user-settable, and data registers will keep their values intact when digital interface (SPI or I2C) is accessed. In addition the data can be pre-processed by digital moving average filter for bandwidth control. Please refer to "Control Registers" for more details on the sampling period and bandwidth control.

A thermometer is embedded in DMARD08. Its temperature sensitivity is 16 LSB/℃ and the central value (0h) stands for 25℃. For example a Tout[10:0] reading of 80h means 25+80h/16=33℃. The acceleration sensitivity is 256 LSB/g and the central value (0h) stands for 0g. For example a Xout[10:0] reading of 100h means 100h/256=1g.

Following lists the summary of sensor output and data registers:

1. Tout[10:0]: 11-bit temperature output, register 00h:bit7~0 + 01h:bit2~0
2. Xout[10:0]: 11-bit X-axis output, register 02h:bit7~0 + 03h:bit2~0
3. Yout[10:0]: 11-bit Y-axis output, register 04h:bit7~0 + 05h:bit2~0
4. Zout[10:0]: 11-bit Z-axis output, register 06h:bit7~0 + 07h:bit2~0

Control Registers

INT1 and INT2 Source Configure

I1CFG[1:0] (08h:bit5, 4) and I2CFG[1:0] (08h:bit7, 6) are interrupt pins (INT×, ×=1, 2) source configuration bits respectively. DMARD08 has two interrupt pins configurable from three interrupt sources of freefall, click and high-G. Each interrupt INT× has two bits to configure its output from any of the three interrupt sources, or alternatively turn it off by grounding. The INTx source configuration table can be found in Table 5.

Table 5: INTx Pin Source Configuration Table

IxCFG[1] x=1, 08h:bit5 x=2, 08h:bit7	IxCFG[0] x=1, 08h:bit4 x=2, 08h:bit6	INTx Source
0	0	GND
0	1	Freefall
1	0	Click
1	1	High-G

Note: x=1, 2

Freefall Interrupt Enable

IxCFG[1:0] has a side effect on the freefall interrupt enable control. If either pin of INTx is configured to source its output from freefall, i.e. IxCFG[1:0] = 01b, the freefall interrupt is automatically

enabled. When the freefall interrupt is enabled, DMARD08 will watch closely the acceleration values of all three axes as compared to some threshold. The INTx pin will directly reflect the comparison result, in other words the result is not latched. The INTx pin will be logic-1 if all three acceleration magnitudes are below the designated threshold value, which potentially indicates a freefall in process. On the other hand, the INTx pin will be logic-0 if any of three acceleration magnitudes rises above the threshold. The freefall interrupt flag (FFInt, 0Ch:bit7) serves the same purpose and manner as the INTx pin. This flag can be read via the SPI/I2C digital interface, and therefore is an alternative to the INTx pin if end users have GPIO constraint. See "Interrupt Status Registers" for details. User can set freefall threshold, see "Freefall Threshold" for details.

High-G Latch Control

HGL (08h:bit3) is the high-G latch control. Under some circumstances the high-G detection event may need to be latched. Logic-1 HGL will cause the high-G detection results latched. See “High-G Detection” for details on high-G detection.

Bandwidth

Tms (08h:bit2) is used to setup the internal ADC sampling period, together with N[1:0] (08h:bit1, 0), which is to setup the digital filtering of ADC output data, to obtain the desired bandwidth. Digital filters can be selectively activated to reduce the bandwidth to as low as 20 Hz. A moving average filter of various lengths is implemented as the digital filter. Please see Table 6 for the sampling period and frequency settable by Tms, and Table 7 for the moving average length settable by N[1:0]. Bandwidth table can be found in Table 8.

Table 6: Sampling Period Table

Tms (08h: bit2)	Sampling Period (ms)	Sampling Frequency (Hz)
0	2.925	342
1	1.462	684

Table 7: Moving Average Length Table

N[1] (08h: bit1)	N[0] (08h: bit0)	Average Order
0	**0**	8
0	**1**	4
1	**0**	2
1	**1**	1

Table 8: Bandwidth Table

Hz		N[1:0] (08h:bit1, 0)			
		00	01	10	11
Tms (08h: bit2)	0	19	38	76	No Filter
	1	38	76	153	

High-G Detection

HGXEn, HGYEn, HGZEn (09h:bit6, 5, 4) are the X-, Y-, and Z-axis high-G interrupt enable control bits respectively. If the respective high-G interrupt enable bit is set to 1, high-G monitoring is enabled for the respective axis. Upon enabled, DMARD08 will check closely if the acceleration magnitude of the respective axis exceeds some high-G threshold value. Furthermore the HGAO (09h:bit7) serves as the logical combination control bit for multiple axial detections. Logic-1 HGAO will do “logic-AND” of enabled multiple axial detections before output to the configured interrupt pin INT×. On the contrary, logic-0 HGAO will do “logic-OR” of enabled multiple axial detections before output to the configured interrupt pin INT×. Logic-1 INT× stands for high-G event detection and logic-0 otherwise. The INTx pin will directly reflect the detection result, in other words the result is not latched. The high-G interrupt flag (HGInt, 0Ch:bit6) serves the same purpose and manner as the INTx pin. This flag can be read via the SPI/I2C digital interface, and therefore is an alternative to the INTx pin if end users have GPIO constraint.

In the case when the enabled multiple axial detections are logic-OR’ed (HGAO is logic-0), we may want to further identify which axis and direction cause the high-G detection. This can be achieved by first latching the result and then checking direction flags. Logic-1 HGL(08h:bit3) will cause the high-G detection results latched. Then high-G direction flags (XHGP, XHGN, YHGP, YHGN, ZHGP, ZHGN, 0Ch:bit5~0) can be checked to detail the high-G axis and direction upon high-G detection. The latch will be automatically cleared after the high-G flag register (0Ch) is read. Following summarizes the meaning when respective flag is set.

1. XHGP: high-G detected in the X-axis positive direction
2. XHGN: high-G detected in the X-axis negative direction
3. YHGP: high-G detected in the Y-axis positive direction
4. YHGN: high-G detected in the Y-axis negative direction
5. ZHGP: high-G detected in the Z-axis positive direction
6. ZHGN: high-G detected in the Z-axis negative direction

Please note that when the enabled multiple axial detections are logic-AND’ed (HGAO is logic-1) the high-G latch (HGL is logic-1) is not supported. The outcome may not be repeatable when HGAO and HGL are both set.

For INT× configuration, see “INT1 and INT2 Source Configure”. User can set respective high-G threshold, see "High-G Threshold" for details. For high-G interrupt and direction flags, see "Interrupt Status Registers" for details. For high-G latch, see “High-G Latch Control” for details.

Click Interrupt Enable

CLXEn, CLYEn, CLZEn (09h:bit2, 1, 0) are the X-, Y-, and Z-axis click interrupt enable control bits respectively. If the respective click interrupt enable bit is set to 1, click monitoring is enabled for the respective axis. DMARD08 will check closely if the respective axis acceleration value double crosses some click threshold. In such case a click event is detected on the way of second cross. On detection the configured INT× pin will be latched to logic-1. The click interrupt flag (CLInt, 0Dh:bit6) serves the same purpose and manner as the INTx pin. This flag can be read via the SPI/I2C digital interface, and therefore is an alternative to the INTx pin if end users have GPIO constraint. Respective click direction flags (XCLP, XCLN, YCLP, YCLN, ZCLP, ZCLN, 0Dh:bit5~0) will also be set to 1 depending on detected axis and direction. The latch will be automatically cleared after the click flag register (0Dh) is read. See "Interrupt Status Registers" for details. For INT× configuration, see “INT1 and INT2 Source Configure”. User can set respective click threshold, see "Click Threshold" for details.

High-G Threshold

HGth[3:0] (0Ah:bit7~4) is the 4-bit high-G threshold control register with 250mg per code. The effective setting range is from 0Ch (3.0g) to 01h (250mg). The default value is 08h (2.0g). See "High-G Interrupt Enable" for high-G detection enable control.

Freefall Threshold

FFth[3:0] (0Ah:bit3~0) is the 4-bit freefall threshold control register with 62.5mg per code. The effective setting range is from 0Fh (937.5mg) to 01h (62.5mg). The default value is 08h (500mg). See "Freefall Interrupt Enable" for freefall detection enable control.

Click Threshold

Clickth[3:0] (0Bh: bit3~0) is the 4-bit click threshold control register with 250mg per code. The effective setting range is from 0Ch (3.0g) to 01h (250mg). The default value is 08h (2.0g). The threshold will be checked against double-cross for click event when the click interrupt enable is set, see "Click Interrupt Enable" for proper register setup. Appropriate flag will be set to 1 upon detecting click event when the INT pin is latched to logic-1, see "Interrupt Status Registers" for details.

Interrupt Status Registers

0Ch and 0Dh serve as the interrupt status registers. When relevant events trigger interrupts, configured INT× pin and appropriate interrupt status bits will be set. For a non-latched interrupt, the interrupt status register can serve as a replica of configured INT×, and accessed from typical digital interface instead of dedicated GPIO. For a latched interrupt, more detailed information is kept in the interrupt status registers for users to further distinguish interrupt sources. The latch will be automatically cleared after appropriate interrupt status register is read.

Freefall Interrupt Flag

FFInt (0Ch:bit7) is the freefall interrupt flag. The freefall interrupt flag serves the same purpose and manner as the configured INTx pin. This flag can be read via the SPI/I2C digital interface, and therefore is an alternative to the INTx pin if end users have GPIO constraint. See “INT1 and INT2

Source Configure", "Freefall Interrupt Enable" and "Freefall Threshold" for proper register setup.

High-G Interrupt Flag

HGInt (0Ch:bit6) is the high-G interrupt flag. The high-G interrupt flag serves the same purpose and manner as the configured INTx pin. This flag can be read via the SPI/I2C digital interface, and therefore is an alternative to the INTx pin if end users have GPIO constraint. See "INT1 and INT2 Source Configure" and "High-G Detection" for proper register setup.

X-axis High-G Flag

XHGP(0Ch:bit5) and XHGN(0Ch:bit4) is the flag for the high-G detection along the X-axis positive and negative direction respectively. XHGP is set when the X-axis acceleration exceeds the positive value of the high-G threshold. Likewise XHGN is set when the X-axis acceleration falls beyond the negative value of the high-G threshold. Please refer to "High-G Detection" for proper register setup.

Y-axis High-G Flag

YHGP(0Ch:bit3) and YHGN(0Ch:bit2) is the flag for the high-G detection along the Y-axis positive and negative direction respectively. YHGP is set when the Y-axis acceleration exceeds the positive value of the high-G threshold. Likewise YHGN is set when the Y-axis acceleration falls beyond the negative value of the high-G threshold. Please refer to "High-G Detection" for proper register setup.

Z-axis High-G Flag

ZHGP(0Ch:bit1) and ZHGN(0Ch:bit0) is the flag for the high-G detection along the Z-axis positive and negative direction respectively. ZHGP is set when the Z-axis acceleration exceeds the positive value of the high-G threshold. Likewise ZHGN is set when the Z-axis acceleration falls beyond the negative value of the high-G threshold. Please refer to "High-G Detection" for proper register setup.

Click Interrupt Flag

CLInt (0Dh:bit6) is the click interrupt flag. The click interrupt flag serves the same purpose and manner as the configured INTx pin. This flag can be read via the SPI/I2C digital interface, and therefore is an alternative to the INTx pin if end users have GPIO constraint. See "INT1 and INT2 Source Configure", "Click Interrupt Enable" and "Click Threshold" for proper register setup.

X-axis Click Flag

XCLP (0Dh:bit5) and XCLN (0Dh:bit4) are X-axis positive and negative direction click flag. The flag will be latched to 1 upon detecting click event along X-axis when the configured INT× pin is latched to logic-1. The X-axis click event is to check double-crossing some click threshold. Depending on the double-crossing direction, positive or negative flag is set respectively. The click event is fired at the second crossing. For example, when the X-axis click enable is set, i.e. CLXEn (09h:bit2) = 1, with default threshold value 2.0g, i.e. Clickth[3:0] (0Bh:bit3~0) = 08h, Figure 5 shows a scenario that the X acceleration first double-cross the positive threshold 2.0g and then secondly double-cross the negative threshold -2.0g. The first double-cross will trigger positive direction click (flag XCLP set to 1) at the second cross. The latter double-cross will trigger negative direction click (flag XCLN set to 1) at the second cross. See "INT1 and INT2 Source Configure", "Click Interrupt Enable" and "Click Threshold" for

proper register setup.

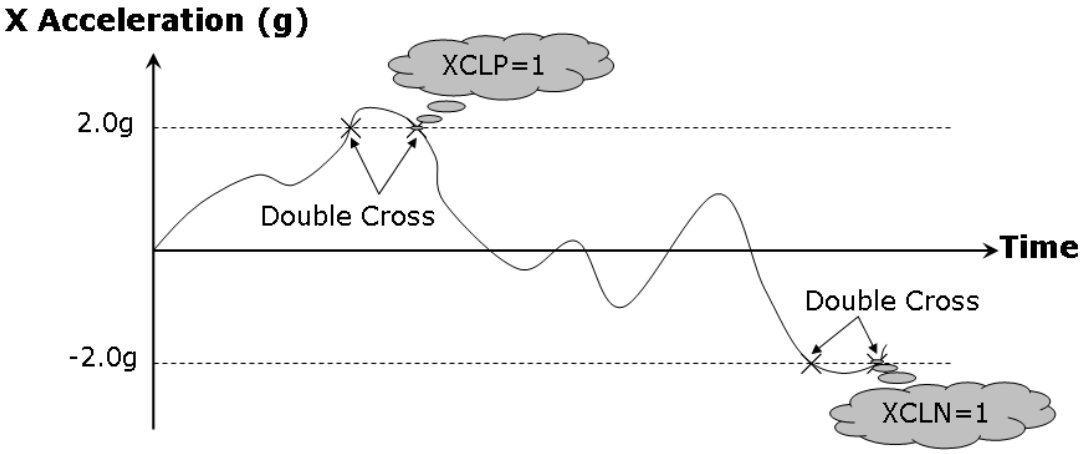


Figure 5: X-axis Click Event Trigger Example

Y-axis Click Flag

YCLP (0Dh:bit3) and YCLN (0Dh:bit2) are Y-axis positive and negative direction click flag. They work in analog to XCLP and XCLN.

Z -axis Click Flag

ZCLP (0Dh:bit1) and ZCLN (0Dh:bit0) are Z-axis positive and negative direction click flag. They work in analog to XCLP and XCLN.

Digital Interface

DMARD08 provides two digital interfaces (SPI 4-wire and I2C) and an interrupt output signal for easy configuration and data/status query. The digital interface can be used to regularly read the data registers of acceleration and temperature output. The DMARD08 can also be configured by setting up proper control registers via the digital interface. For example, the interrupt pin can be configured to response to freefall or click event. Upon triggered interrupt, user can use the digital interface to check the interrupt status register for proper interrupt source verification.

I2C Interface

DMARD08 includes a slave I2C interface. CS must be connected to ground when choosing I2C as digital interface. The I2C bus takes master clock through SCL pin and exchanges serial data via SDI. SDI is bidirectional (input/output) with open drain. It must be connected externally to VIF via a pull-up resistor. SDO is used to set I2C slave address SDO-bit. The SDO-bit can be set to 1 by connecting SDO to VIF, or to 0 by grounding.

I2C Slave Address

DMARD08 has a 7-bit slave address. The six high bits is fixed at value 001110b. The LSB of slave address (bit1 or SDO-bit) can be set to either 1 or 0 by physical SDO connection. For example if SDO is connected to high (VIF), the 7-bit slave address is 0011101b, and vice versa. Additional RW bit sets the chip in read or write mode, RW = 0 for write and 1 for read. Table 8 summaries the I2C slave address and RW.

Table 9: I2C slave address & RW

Slave Address							bit0 (RW)	Hex	Read/Write
bit7	bit6	bit5	bit4	bit3	bit2	bit1 (SDO-bit)			
0	0	1	1	1	0	0	0	38h	Write
						0	1	39h	Read
						1	0	3Ah	Write
						1	1	3Bh	Read

I2C Access Format

Data transfer begins by bus master indicating a start condition (ST) of a falling edge on SDI when SCL is high. Stop condition (SP) also indicated by bus master is a rising edge on SDI when SCK is high.

After a start condition, the slave address + RW bit must be sent by master. If the slave address does not match with DMARD08, there is no acknowledge and the following data transfer will not affect DMARD08. If the slave address corresponds to DMARD08, it will acknowledge by pulling SDI to low and the SDI line is let free enabling the data transfer. The master should let the SDI high (no pull down) and generate a high SCL pulse for DMARD08 acknowledge.

Table 10: I2C access format

Single Write

ST	Slave Address + RW	A	Reg Address	A	Data	A	SP

Multiple Write

ST	Slave Address + RW	A	Reg Address	A	Data	A	Data	NA	SP

Single Read

ST	Slave Address + RW	A	Reg Address	A	SR	Slave Address + RW	A
Data	NA	SP					

Multiple Read

ST	Slave Address + RW	A	Reg Address	A	SR	Slave Address + RW	A
Data	A	Data	NA	SP			

Master to Slave Slave to Master

A = acknowledge (SDA Low)
NA = not acknowledge (SDA High)
ST = START condition
SR = repeated START condition
SP = STOP condition

I2C Specifications

Table 11: I2C Timing Specification

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SCL clock frequency	SCL	—	—	400	kHz
Clock low period	t_{LOW}	1.2	—	—	μs
Clock high period	t_{HIGH}	0.6	—	—	μs
Bus free to new start	t_{BUF}	1.2	—	—	μs
Start hold time	$t_{HD.STA}$	0.6	—	—	μs
Start setup time	$t_{SU.STA}$	0.6	—	—	μs
Data-in hold time	$t_{HD.DAT}$	0	—	—	μs
Data-in setup time	$t_{SU.DAT}$	100	—	—	ns
Stop setup time	$t_{SU.STO}$	0.6	—	—	μs
Data-out hold time	t_{DH}	50	—	—	ns

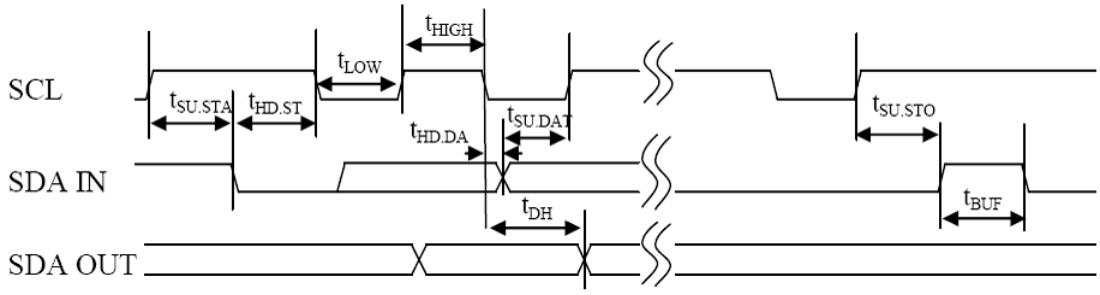


Figure 6: I2C Timing Diagram

SPI Interface

The SPI interfaces using four-wire bus provide 22-bit protocols. Multiple read/write is supported.

The communication starts with a read/write (R/W) control bit with R/W equals 0 for writing or 1 for reading. Following the R/W control bit comes a 13-bit address and an 8-bit data for single read/write, as shown in Figure 7 & 8. To read 11-bit acceleration and temperature data, the SPI interface provides an option to use the multiple read commands to read more than one byte. This is activated when the serial enable pin CS stays active high after the read out of a data register, as shown in 9 & 10.

CS is active high. Data on SDI is latched by DMARD08 at SCL rising edge and the SDO changes state at SCL falling edge. Communication starts when CS goes to high and stops when CS goes to low. During these transitions on CS, SCL must be high.

SPI Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit
CS setup time	t_{s0}	300	—	—	ns
Data setup time	t_{s1}	150	—	—	ns
CS hold time	t_{h0}	150	—	—	ns
Data hold time	t_{h1}	150	—	—	ns
SCL pulse low width	t_{w1L}	160	—	—	ns
SCL pulse high width	t_{w1H}	160	—	—	ns
CS pulse low width	t_{w2}	1	—	—	μs

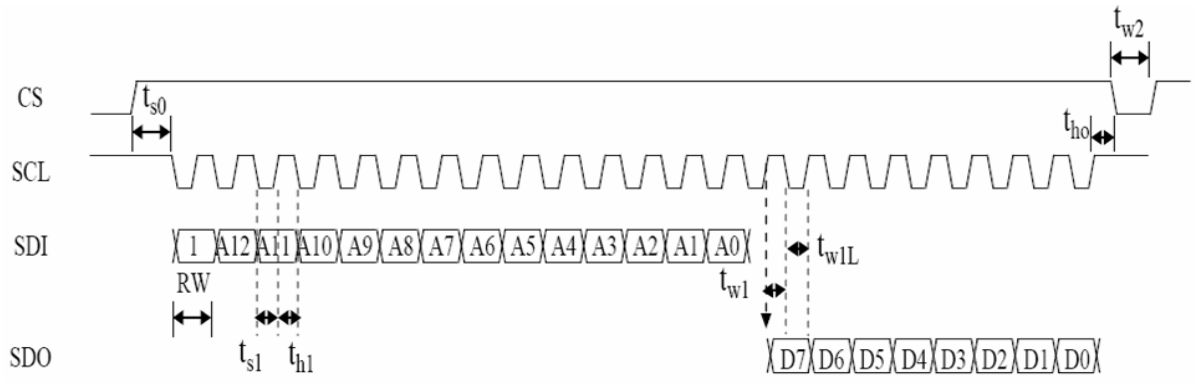


Figure 7: SPI Single Read

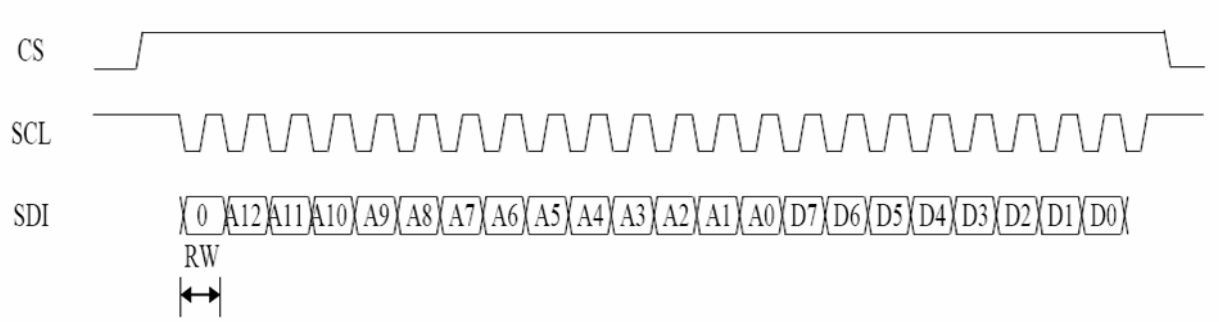


Figure 8: SPI Single Write

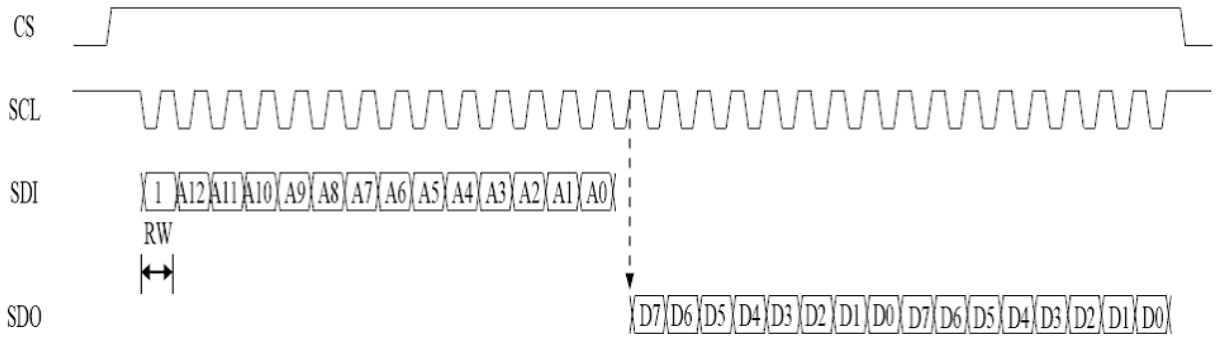


Figure 9: SPI Multiple Read

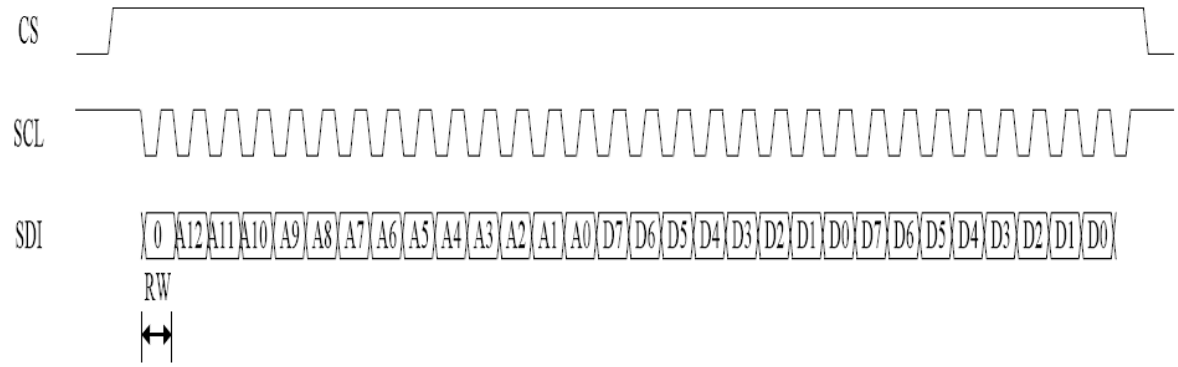


Figure 10: SPI Multiple Write

Package

Outline Dimension

Unit: mm

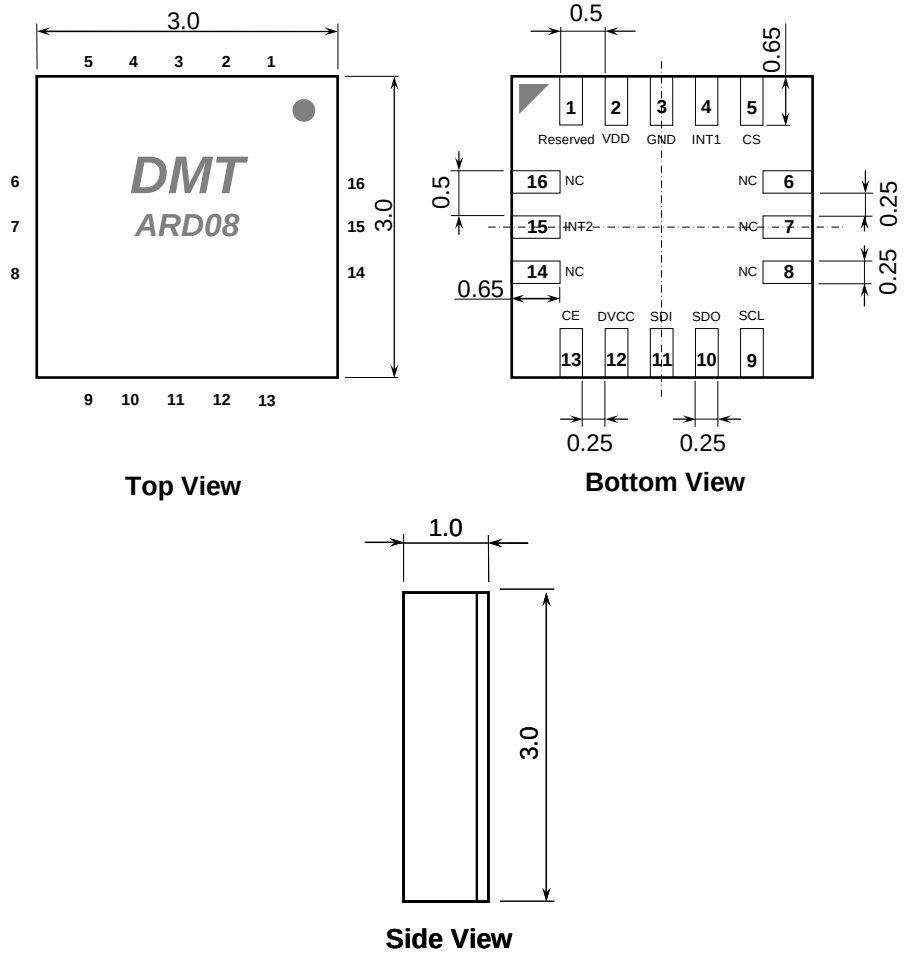


Figure 11: Package Outline Dimension

Axes Orientation

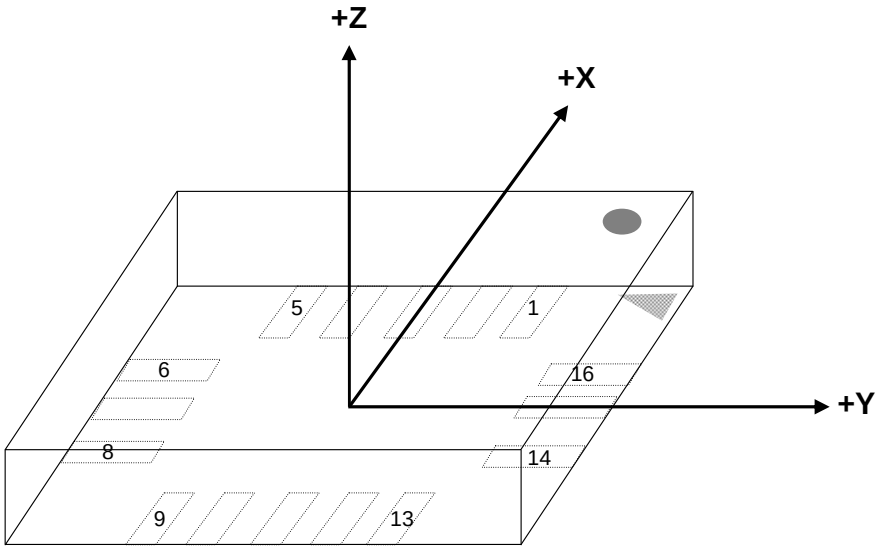


Figure 12: Axes Orientation of DMARD08

RoHS Compliance

The 16-pin LGA package conforms to the EU directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment 2002/95/EC.

Surface Mounting Information

The accelerometer is a delicate device that is sensitive to the mechanical and thermal stress. Proper PCB board design and well-executed soldering processes are crucial to ensure consistent performance. A recommended land pad layout can be found in the Figure 13. For more SMT information, please refer to application note “AN004: SMT Guide for Accelerometer in LGA Package”.

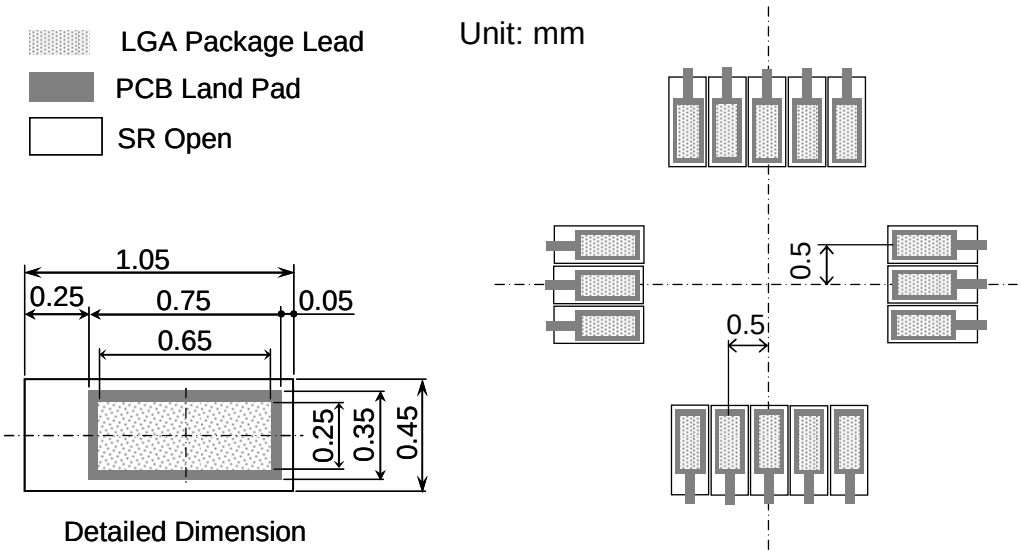


Figure 13: Layout Recommendation for PCB Land Pad and SR Open

Document History and Modification

Revision No.	Description	Date
Rev1.0	First release	2011/8/1

Domintech Co., Ltd. Tel: +886-2-2290-1288 Fax: +886-2-2290-1266 http://www.domintech.com.tw